

### TECHNISCHE UNIVERSITÄT IN DER KULTURHAUPTSTADT EUROPAS CHEMNITZ

## MEMS-based Fingerprinting Architecture for Trustworthy Electronics

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**Internet of things (IoT):** network of all production systems and



#### Integration of a Micro-Electro-Mechanical System (MEMS)

their modules  $\rightarrow$  Digitization of process chains

• Increase of process performance, quality and functionality • Decrease of energy consumption and operation costs

Modules are vulnerable to manipulation. Possibilities for attack increase with increasing complexity (especially in a global value chain).

Aim

as physical unclonable function (PUF) in system modules

- Clear identifiability of modules
- Protection against manipulation and unauthorized replacement of original components
- Concepts for integration into architecture and key generation

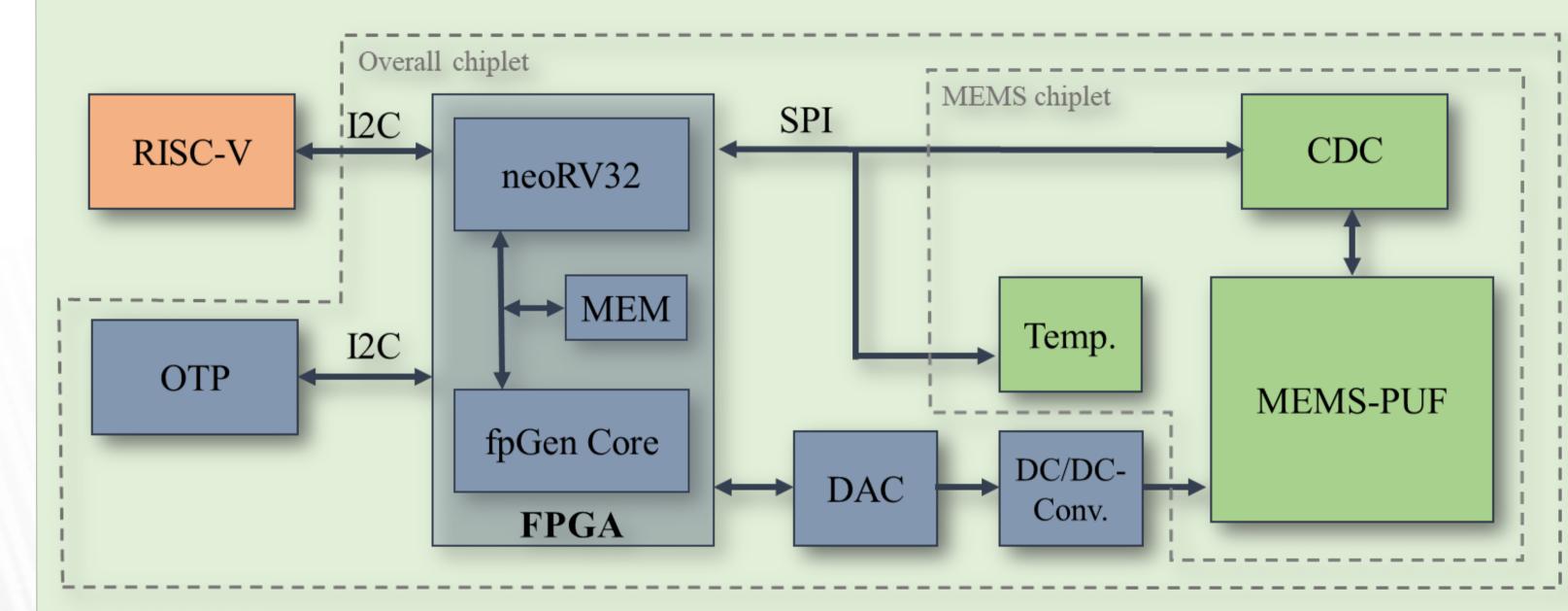
#### **Trusted Execution Environment (TEE) (orange)** URE • RISC-V = representative of interrogating electronics • Fingerprint device is one entity of TEE ECT ARCHITI **MEMS chiplet (green):** • Specific MEMS component (MEMS-PUF)

• MEMS-related electronics

#### **Fingerprint electronics (blue):**

• FPGA and peripherals for controlling and evaluating the MEMS chiplet

#### System architecture



Legend: One time programmble (OTP), Capacitance-to-Digital Converter (CDC), Memory (MEM), Fingerprint generator IP Core (fpGen Core), Field Programmable Gate Array (FPGA), Digital-to-Analog Converter (DAC)

MEMS

ΥST

 $\mathbb{Z}$ 

**Design scheme SEM image of fabricated MEMS** Var 04 Var 01

#### Specific design for PUF application

- Implementation of MEMS, which are inherently prone to scattering/technological tolerances by design
- Focus: Robust design, simple signal detection  $\rightarrow$  MEMS varactor array, capacity values used for fingerprinting  $\rightarrow$  Forcing of technological spread by special design MEMS technology: BDRIE – Bonding and Deep Reactive Ion Etching (Full-Silicon)

#### **MEMS varactor array**

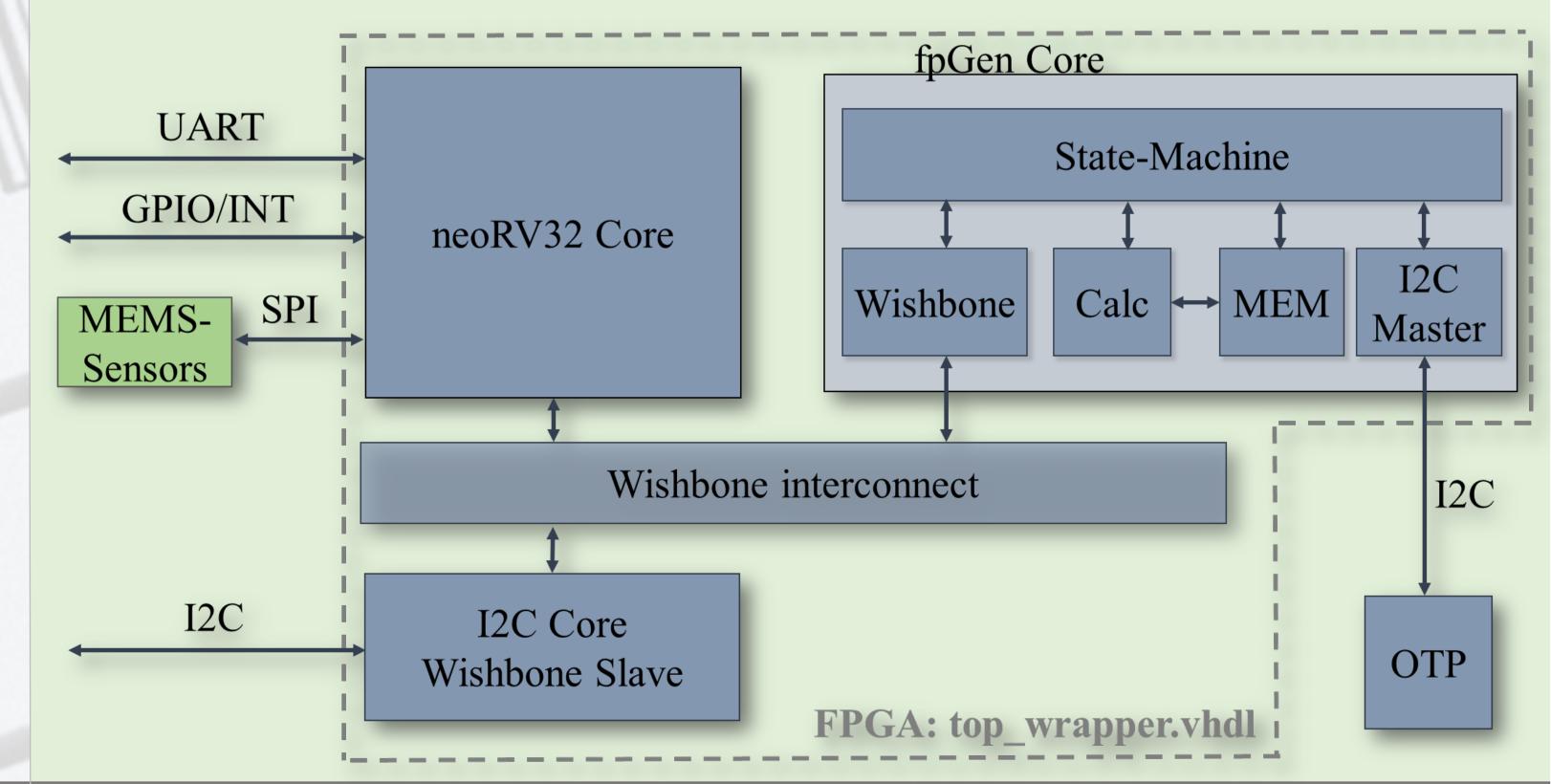
• Chip size: 5.1 x 5.1 mm<sup>2</sup>, 16 separate capacities (4 main, 4 sub designs) • No absolute trends  $\rightarrow$  Basically all designs the same, base capacity identical • Design variations: Direction, comb geometry, gap spacing, system stiffness

# RONICS

#### neoRV32 microcontroller

- Open source IP-Core, central control unit
- Provides the connection to RISC-V and MEMS-Chiplet
- Readout of CDC and temperature sensor

#### **Fingerprint electronics architecture**



FINGERPRINT

Read/configuration of DAC for MEMS driving

#### **Fingerprint generation Core**

Förderkennzeichen

16ME0243K - 16ME0254

 Carries out a cyclic fingerprint generation Compares fingerprint with a hashed value in OTP

#### **I2C Core**

Communication with Trusted Execution Environment (RISC-V)

VIDES



Bundesministerium für Bildung und Forschung

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