VE-VIDES

Designmethoden und HW/SW-Co-Verifikation für die eindeutige Identifizierbarkeit von Elektronikkomponenten

Developing Trustworthy Automotive Integrated Circuits

Enkele Rama, Mouadh Ayache, Louei Nefzi, Stefan Simon, Christian Malter, Saleh Mulhem, Matthias Korb, Mladen Berekovic

Universität der Bundeswehr München

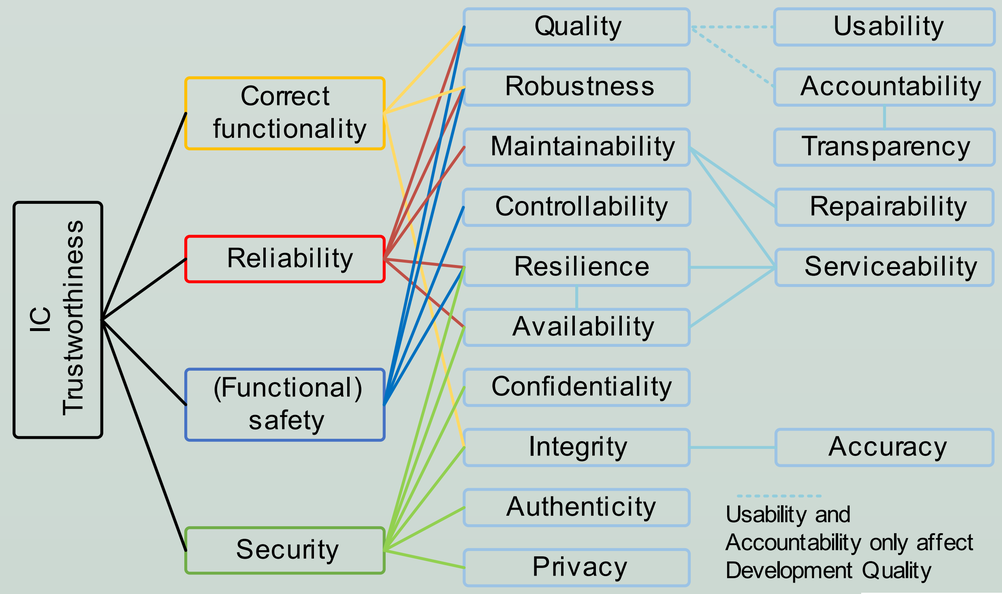
UNIVERSITÄT ZU LÜBECK
INSTITUT FÜR TECHNISCHE INFORMATIK

GEFÖRDERT VOM
Bundesministerium für Bildung und Forschung

CARIAD SYNOPSYS®

Trustworthy Automotive Integrated Circuits

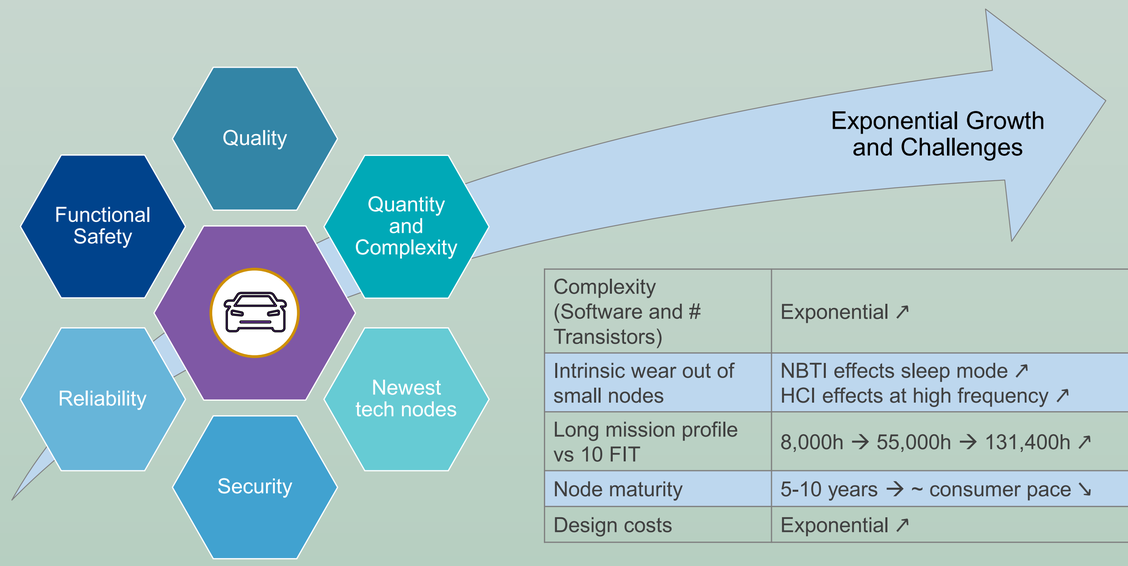
- AP5 Goal: Improve the trustworthiness of **automotive semiconductors**
- Defined what **trustworthiness** means in the context of **integrated circuits**
- Identified **critical issues** that undermine IC trustworthiness
- Identified **critical requirements** for trustworthy automotive ICs
- Defined trustworthy **development flows** for design, verification, functional safety, DFT insertion, and security
- Defined **key checks, metrics, reports and milestones** necessary for assessing the trustworthiness of automotive ICs
- Defined use-cases for **SLM monitors** to enhance IC trustworthiness
- Defined a **metric** for evaluating the **risk** an issue represents to trustworthiness of ICs



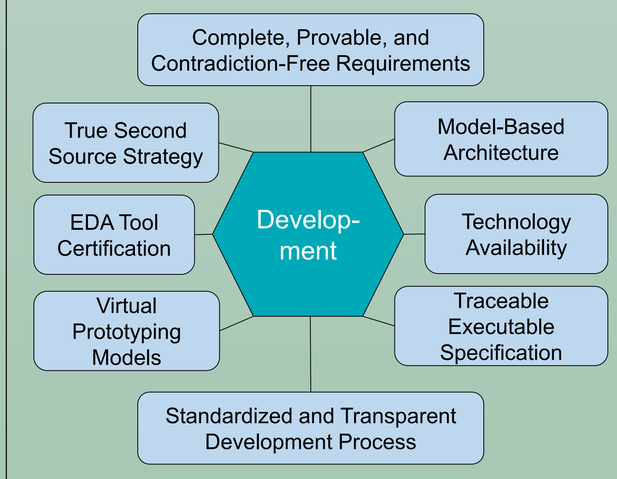
"Trustworthy Integrated Circuits: From Safety to Security and Beyond"
An IEEE Access Journal Article

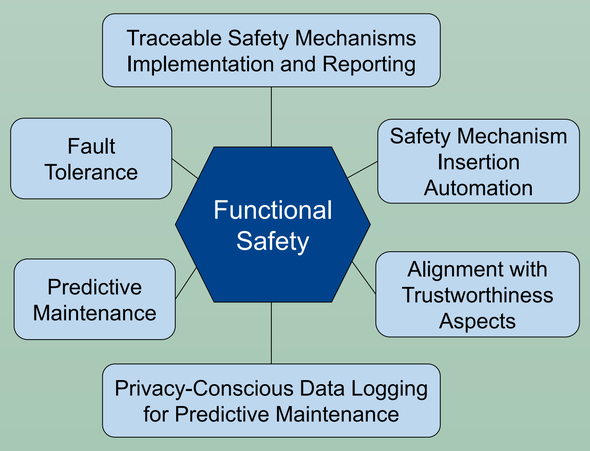
Requirements and Best Practices for Trustworthy Automotive Semiconductors

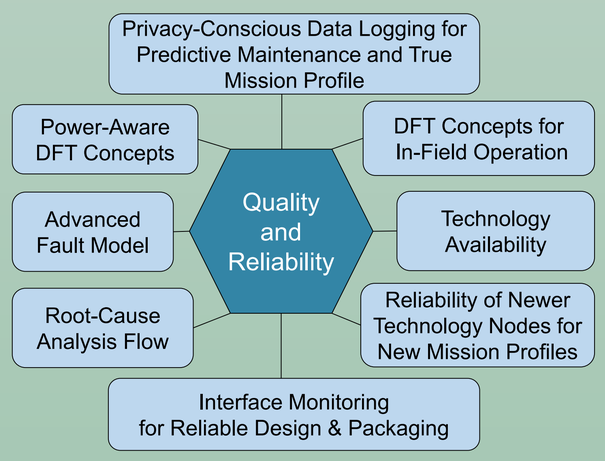
- **Complexity** of electronic systems in ADAS, HAD, and in-vehicle infotainment is growing exponentially
- Transition from domain-specific ECUs to zonal architecture necessitates **high-performance computing**
- New use cases for BEVs introduce significant **design challenges**
- **Critical requirements** to enable trustworthy development of automotive semiconductors with a focus on **quality**, **functional safety**, **reliability**, and **security**
- **Best practices** via EDA tools throughout the development flow to fulfill these requirements

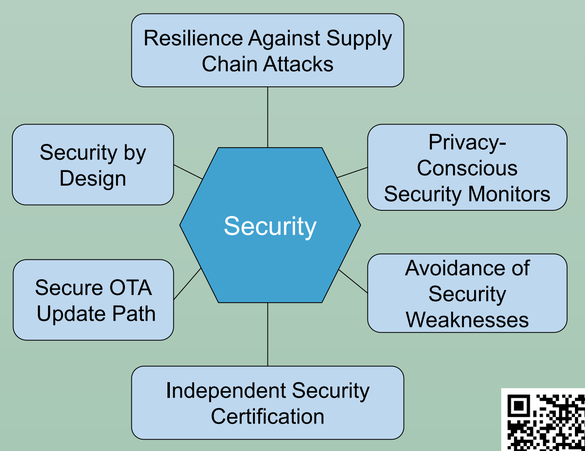


Complexity (Software and # Transistors)	Exponential ↗
Intrinsic wear out of small nodes	NBTI effects sleep mode ↗ HCI effects at high frequency ↗
Long mission profile vs 10 FIT	8,000h → 55,000h → 131,400h ↗
Node maturity	5-10 years → ~ consumer pace ↘
Design costs	Exponential ↗





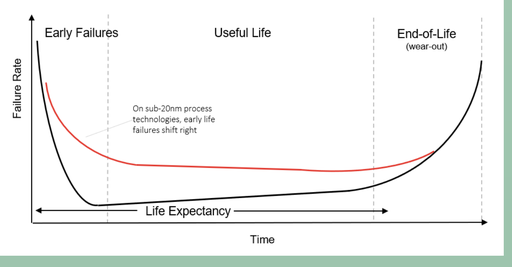




"Requirements and Best Practices for Trustworthy Automotive Semiconductors"
A White Paper by AUDI, CARIAD and Synopsys

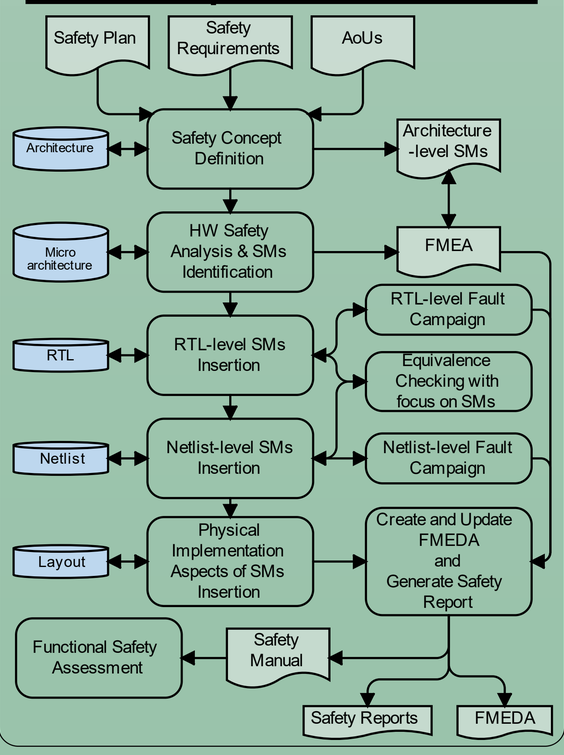
Monitoring Use-Cases

Aging & Reliability

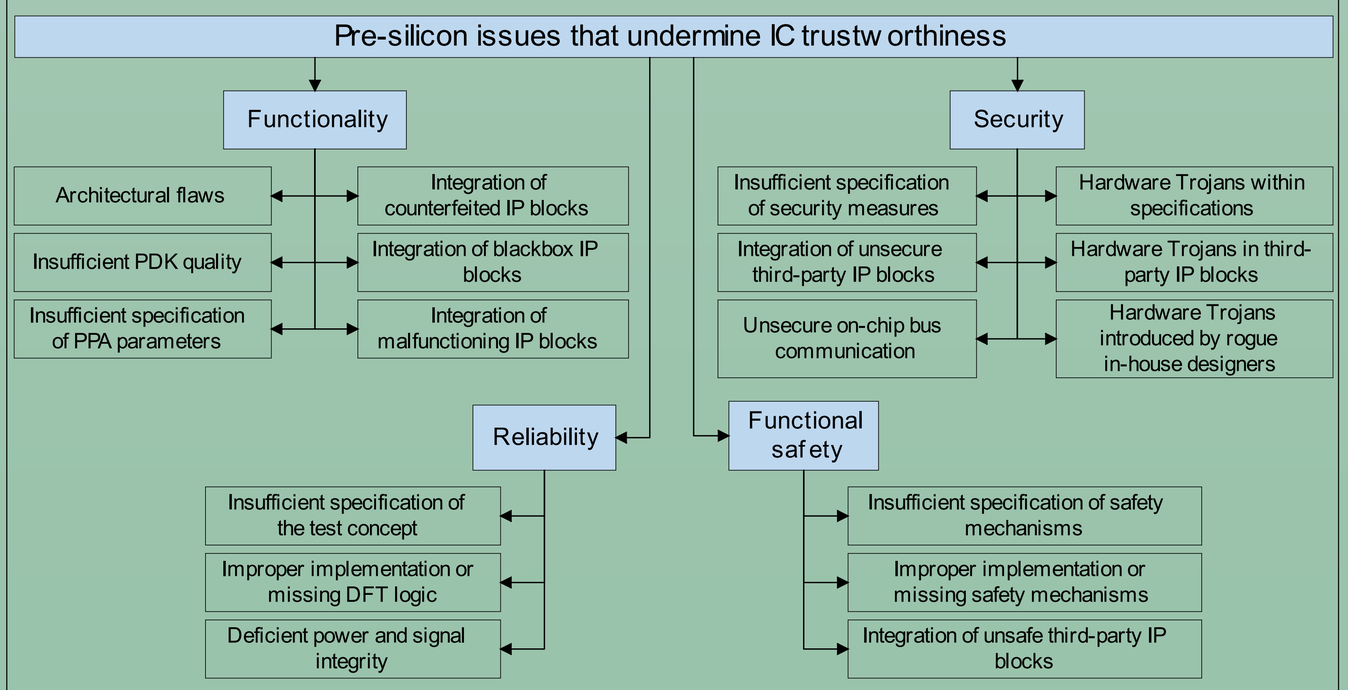


Predictive Maintenance

Development Flows



Trustworthiness Issues



BOSCH CARIAD Fraunhofer IIS IMMS Infineon SYNOPSYS® SIEMENS DLR OFFIS INSTITUT FÜR INFORMATIK TECHNISCHE UNIVERSITÄT CHEMNITZ universität ulm xfab

Projektkoordination:
Infineon Technologies AG
Djones Lettnin
fon +49 89 234 89 730
e-mail: Djones.Lettnin@infineon.com

Projektmanagement:
edacentrum GmbH
Ralf Popp
fon +49 511 9368 7464
e-mail: popp@edacentrum.de

Laufzeit: 01.03.2021 - 28.02.2024
Homepage: www.edacentrum.de/ve-vides/

Bundesministerium für Bildung und Forschung

Das diesem Beitrag zugrunde liegende Vorhaben wurde mit Mitteln des Bundesministeriums für Bildung und Forschung unter den Förderkennzeichen 16ME0243K - 16ME0254 gefördert.